

OV511⁺

*Advanced Camera to USB Bridge
OmniVision Technologies, Inc.
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Data Sheet Rev. 1.2



2 Architecture

2.1 General Description

OV511⁺ based on OV511, is a low cost and highly integrated solution for USB PC camera applications. It remains OV511's performance unchanged or is improved, while some new features were implemented. New features include built-in USB transceiver with selectable external USB transceiver interface, more effective packet size of the isochronous pipe, programmable LED control, programmable switching power clock with frequencies of 24K/48K/96K/192KHz, etc.

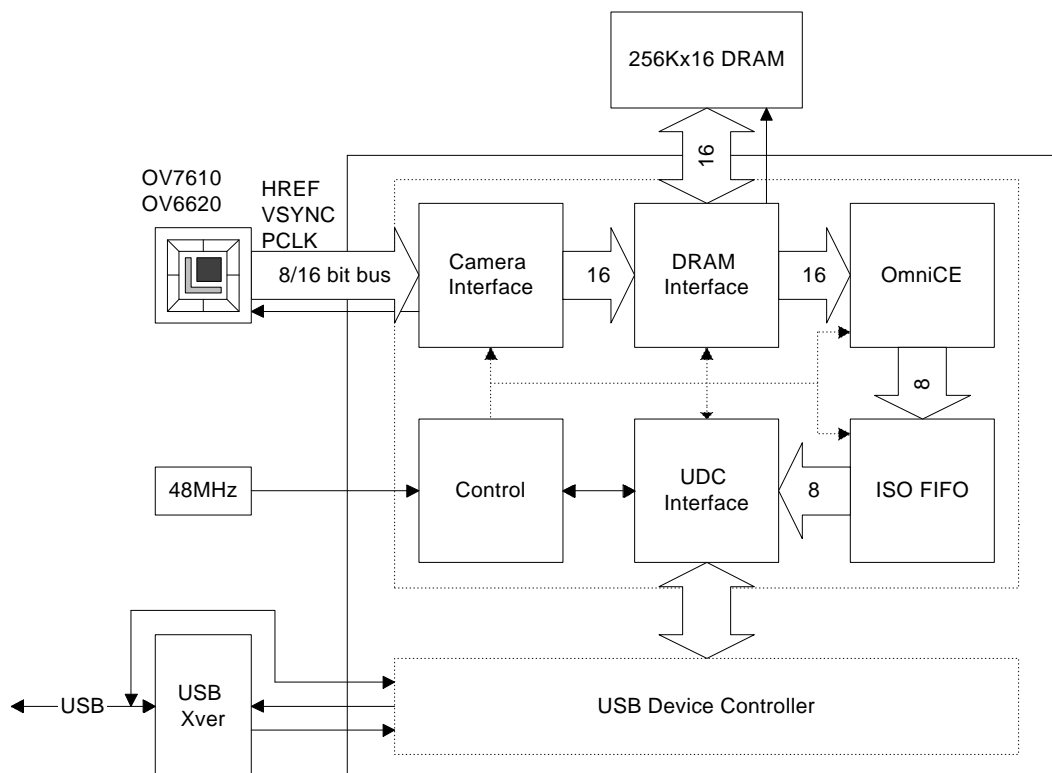
OV511⁺ is a USB PC camera controller that includes a proprietary compression engine supporting real time image transfer through USB bus. A complete USB camera system consists of OV511⁺, a 256Kx16 EDO DRAM, and a digital camera such as OV7620 for VGA resolution or OV6620 for CIF resolution.

Camera Interface generates different image formats by taking either 16-bit YUV 4:2:2/RGB raw data or 8-bit Y 4:0:0/RGB raw data inputs. OmniCE is the proprietary compression engine. It not only performs 10~15fps for VGA and 30fps for CIF, but also allows very fast decompression with low CPU utilization.

Snapshot button allows users to take a high quality, VGA resolution uncompressed still image.

The functional blocks of OV511⁺, as shown in the following figure, consist of Camera Interface, DRAM Interface, OmniCE, UDC interface, ISO FIFO, System Control, SCCB and PIO.

Figure 1. Functional Block Diagram

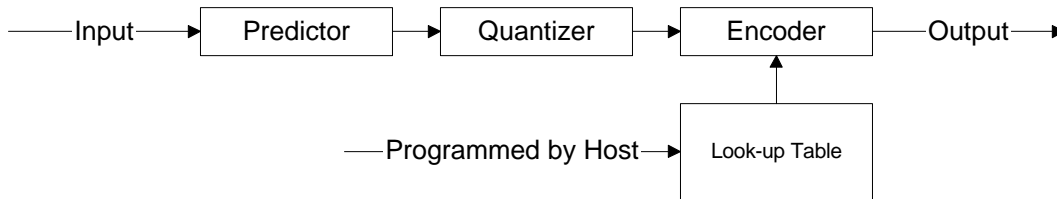


2.2.3 OmniCE

OmniCE is a proprietary compression engine, constructed by the predictor, the quantizer, as well as encoder along with look-up tables. The predictor predicts image pixels horizontally and vertically. The look-up table can be programmed by the software driver according to calculation of probability.

The compression ratio of OmniCE varies from 4 to 8, depending on image complexity. Parameters can be modified dynamically by the software driver to achieve the desired frame rate. It can also be disabled and bypass uncompressed data.

Figure 9. Structure of OmniCE



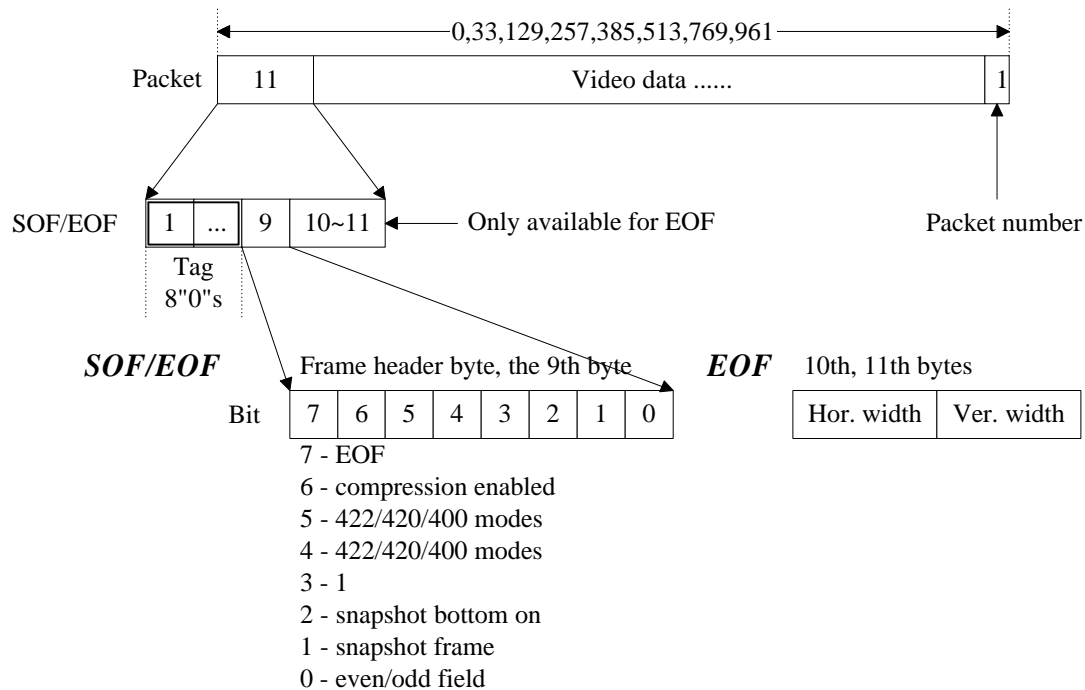
2.2.4 ISO FIFO

OV511+ implements one isochronous endpoint for video data transfer. The available alternates include packet size of 0, 33, 129, 257, 385, 513, 769 & 961. The corresponding ISO FIFO size has to be set by the software driver right before the current alternate is set. The size of ISO FIFO is configurable from 32 to 960 in increment of 32.

Moreover, in order to assist packet reordering in the host, a packet number inserted at the end of each packet can be turned on. An image frame starts with the SOF packet (Start Of an image Frame), while ends with the EOF packet (End Of an image Frame). The packet number counts up from 01 to 255 and back to 01. Only the SOF packet uses the packet number 00.

SOF/EOF packets are indicated by the unique combination which the 1st to the 8th byte are all "0"s and the 9th byte contains a non-zero header. This header contains image information, such as the operating mode, snapshot flag & even/odd field. In the case of the EOF packet, the 10th and 11th bytes also contain the image width and height information.

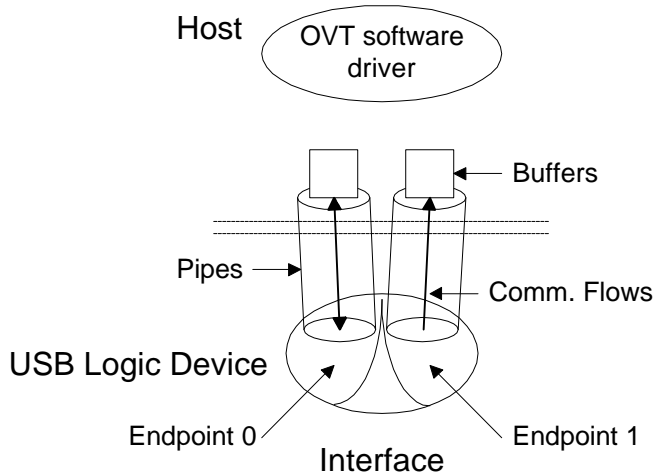
Figure 10. SOF/EOF Formats



2.2.7 USB Device Controller

The camera system constructed by OV511⁺ is defined as a “high-power, bus-powered” USB device. It means that the camera system draws over one and a maximum of five unit loads from the USB cable. Two endpoints are implemented for communication flows between the USB camera device and the USB host. Endpoint 0 is an In-Out type CONTROL endpoint which is the pipe of Descriptors, Configurations and Vendor Commands (internal registers). Endpoint 1 is an In type Isochronous endpoint which is the pipe of video streams.

Figure 12. USB Communication Flow



The USB Descriptors are configured as one configuration, one interface and eight alternates. The packet sizes of eight alternates are 0, 33, 129, 257, 385, 513, 769 & 961.

5 Register Table (Vendor Commands)

5.1 CAMERA INTERFACE

Table 11. Camera Interface Register List

Register Address	Register Name	R/W	Function	Default Value
10h	DLYM[1:0]	RW	Bit 1~0 : Delay modes of video input signals 00 : no delay 01 : delays YUV by one PCLK 10 : delays HREF by one PCLK 11 : delays YUV and HREF by one PCLK	00h
11h	PEM[0]	RW	Bit 0 : Edge modes of PCLK 0 : PCLK negative edge latches video data 1 : PCLK positive edge latches video data	01h
12h	PXCNT[6:0]	RW	Bit 6~0 : Clamped pixel number It defines the clamped pixel number of a horizontal line in increment of 8 pixels. If the pixel number from camera is larger than this number, the spare pixels will be dropped. Clamped Pixel No. = (PXCNT + 1) * 8	27h
13h	LNCNT[6:0]	RW	Bit 6~0 : Clamped line number It defines the clamped line number in increment of 8 lines. If the line number from camera is larger than this number, the spare lines will be dropped. Clamped Line No. = (LNCNT + 1) * 8	1Dh
14h	PXDV[1:0]	RW	Bit 1~0 : Pixel divisor It defines down sampling frequency in the horizontal pixel direction. 00 : divided by 1 01 : divided by 2 10 : divided by 4 11 : divided by 8	01h
15h	LNDV[1:0]	RW	Bit 1~0 : Line divisor It defines down sampling frequency in the vertical line direction. Uses these register bits along with register bit LSTR to retain even or odd lines. 00 : divided by 1 01 : divided by 2 10 : divided by 4 11 : divided by 8	01h
16h	M400[0]	RW	Bit 0 : 8 bit (Y channel only) / 16 bit (Y & UV channels) data input select 0 : 8 bit data in Y channel (UV channel is ignored) 1 : 16 bit data in both Y & UV channels. Uses this register bit along with register bit M420 to select 422/420 formats.	01h
17h	LSTR[0]	RW	Bit 0 : Reserved lines for downing sampling 0 : even lines (2, 4, 6, 8,) 1 : odd lines (1, 3, 5, 7,)	00h
18h	M420[1] YFIR[0]	RW	Bit 1 : YUV422/420 0 : YUV 4:2:2 1 : YUV 4:2:0 Bit 0 : Y channel low pass filter 0 : disabled 1 : enabled	00h

- **Snapshot Operation** – a full set of camera interface registers are duplicated for hardware snapshot operation. These registers replace the normal ones for taking snapshot frame so that the snapshot frame can be different settings from normal frame. The followings are the snapshot registers.

Camera Interface Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
19h	SPDLY[7:0]	RW	Bit 7~0 : Captured frame for snapshot It defines which frame (one frame only) after snapshot function is triggered will be captured. 00000000 : the first frame 10000001 ~ 11111111 : the 2 nd ~ 128 th frame	00h
1Ah	SNPX[6:0]	RW	Bit 6~0 : Clamped pixel number for snapshot	4Fh
1Bh	SNLN[6:0]	RW	Bit 6~0 : Clamped line number for snapshot	1Dh
1Ch	SNPD[1:0]	RW	Bit 1~0 : Pixel divisor for snapshot	00h
1Dh	SNLD[1:0]	RW	Bit 1~0 : Line divisor for snapshot	01h
1Eh	SN400[0]	RW	Bit 0 : 8/16 bit data input for snapshot	01h
1Fh	SNALSTR[2] SN420[1] SNYFIR[0]	RW	Bit 2 : Reserved lines for down sampling for snapshot Bit 1 : YUV422/420 for snapshot Bit 0 : Y channel low pass filter for snapshot	04h

5.2 DRAM INTERFACE

Table 12. DRAM Interface Register List

Register Address	Register Name	R/W	Function	Default Value
20h	ENFC[0]	RW	Bit 0 : Image flow control 0 : disabled, doesn't guarantee a complete image frame 1 : enabled, guarantees a complete image frame	01h
21h	ARCP[0]	RW	Bit 0 : Auto read cycle predictor It predicts the number of read cycles that will be inserted besides write cycles. 0 : disabled, use register bit MRC for manual setting 1 : enabled	01h
22h	MRC[3:0]	RW	Bit 3~0 : Manual read cycle insertion It defines the number of read cycles that will be inserted besides write cycles. Read cycles = MRC + 1	01h
23h	RFC[5:0]	RW	Bit 5~0 : Refresh counter	1Ah

5.3 ISO FIFO

Table 13. ISO FIFO Register List

Register Address	Register Name	R/W	Function	Default Value
30h	PKSZ[4:0]	RW	Bit 4~0 : Packet size It defines the packet size of ISO FIFO which is available from 00000 (0 bytes) to 11110 (960 bytes). The packet size must match with the current alternate setting. Packet size = (32 * PKSZ) bytes	08h
31h	NZPK[3] ENPKNO[1] ENCE[0]	RW	Bit 3 : Zero packet inserted after EOF (image end of frame flag) 0 : disabled 1 : enabled Bit 1 : Packet No. insertion It inserts one extra byte at the end of each packet as the packet number. It counts in sequence, but only the packet containing SOF (image start of frame flag) uses "00". 0 : disabled 1 : enabled Bit 0 : Compressed data non-zero (01) insertion It inserts "01" at the 7 th byte of the packet if the 1 st ~8 th incoming compressed data are all "00". 0 : enabled 1 : disabled	03h

5.4 PIO

Table 14. PIO Register List

Register Address	Register Name	R/W	Function	Default Value
38h	ENPIO[7] PIORW[6] PADD[5:0]	W	Bit 7 : Parallel IO operation 0 : disabled 1 : enabled. UV channel changes to output mode for parallel IO operation. Register bits PADD[5:0] output to pin UV[5:0]. UV[6] performs as OEB, while UV[7] performs as WEB. Y channel is bi-directional. The direction depends on read/write operation of PIO. The bus cycle is executed once only after USB host write to this register and ENPIO = 1. Write data has to be placed in register bits PDATA[7:0] before launching the PIO write cycle. Read data is returned in register bits PDATA[7:0] after launching the PIO read cycle. Bit 6 : Read/write cycle for PIO operation 0 : read cycle 1 : write cycle Bit 5-0 : address port of PIO operation	00h
39h	PDATA[7:0]	RW	Bit 7-0 : data port of PIO operation	00h
3Eh	ENTP[3] TPS[2:0]	W	Bit 3 : BIST operation for OV511 ⁺ 0 : disabled 1 : enabled Bit 2-0 : BIST functions select	00h

- **PIO R/W sequence examples**

Write cycles

1. Writes to data port (PDATA, register 39h)
2. Enables PIO (ENPIO, register 38h), sets up address (PADD, register 38h), & selects write cycle (PIORW, register 38h)
3. Disables PIO (ENPIO, register 38h)

Read cycles

1. Enables PIO (ENPIO, register 38h), sets up address (PADD, register 38h), & selects read cycle (PIORW, register 38h)
2. Reads from data port (PDATA, register 39h)

5.5 SCCB

Table 15. SCCB Register List

Register Address	Register Name	R/W	Function	Default Value
40h	TMOUT[2] NOACK[1] IDLE[0]	R	Bit 2 : Time out flag for SCCB operation. Sets when timer reaches the value set by register bits TMO[4:0]. Bit 1 : No acknowledge on SCCB bus. It's valid when register bit IDLE is set. Bit 0 : SCCB bus idle flag	00h
40h	ENABORT[4] TYPE[2:1] STARTSCCB[0]	W	Bit 4 : Aborts SCCB bus cycle if SCCB slave doesn't response (no acknowledge) Bit 2-1 : Types of SCCB read/write sequence 00 : 3 byte write cycle, in sequence of slave ID (SID), sub address (SWA) & SCCB data (SIO-0) 01 : 2 byte write cycle, in sequence of slave ID (SID) & sub address (SMA) 1x : 2 byte read cycle, in sequence of slave ID (SRA) & SCCB data (SIO-0) Bit 0 : Launches a new SCCB bus cycle if set SCCB won't launch a new cycle if it doesn't finish the previous bus cycle.	00h

SCCB Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
41h	SID[7:0]	RW	Bit 7~0 : SCCB slave ID for 3 or 2 byte write cycles	00h
42h	SWA[7:0]	RW	Bit 7~0 : Sub address for 3 byte write cycles	00h
43h	SMA[7:0]	RW	Bit 7~0 : Sub address for 2 byte write cycles	00h
44h	SRA[7:0]	RW	Bit 7~0 : Slave ID for 2 byte read cycles	00h
45h	SIO-0[7:0]	RW	Bit 7~0 : SCCB read/write data port	00h
46h	PSC[7:0]	RW	Bit 7~0 : SCCB clock prescaler It defines prescaler values for SCCB clock. SCCB bit rate = 93.5 KHz / (PSC + 1)	00h
47h	TMO[4:0]	RW	Bit 4~0 : Time out counter A timer starts to count SCCB clocks when SCCB bus cycle is launched. When the timer reaches TMO, TMOUT is set.	00h

- Snapshot Operation** - During the period of hardware snapshot operation, OV511⁺ first launches a 3 byte SCCB write cycle to SCCB slave device, such as camera, by using register 48h and 49h. It permits SCCB slave device to modify the internal settings before taking the snapshot.

SCCB Register List (continued)

Register Address	Register Name	R/W	Function	Default Value
48h	SPA[7:0]	W	Bit 7~0 : Sub address of the SCCB write cycle for snapshot operation	00h
49h	SPD[7:0]	W	Bit 7~0 : Data port of the SCCB write cycle for snapshot operation	00h

- SCCB R / W Sequence Examples**

Setup stage

- Writes to slave ID (SID, register 41h)

3 byte write cycles

- Writes to sub address (SWA, register 42h)
- Writes to data port (SIO-0, register 45h)
- Writes to control bits to select write cycle and launch SCCB cycles (TYPE, STARTSCCB, register 40h)

2 byte dummy write cycles (In order to set sub address of SCCB slave device for the next coming read cycle)

- Writes to sub address (SMA, register 43h)
- Writes to control bits to select write cycle and launch SCCB cycles (TYPE, STARTSCCB, register 40h)

2 byte read cycles

- Writes to sub address (SRA, register 44h)
- Writes to control bits to select read cycle and launch SCCB cycles (TYPE, STARTSCCB, register 40h)
- Reads from status bits (TMOUT, NOACK, IDLE, register 40h)
- Reads from data port (SIO-0, register 45h)

5.6 SYSTEM CONTROL

Table 16. System Control Register List

Register Address	Register Name	R/W	Function	Default Value
50h	RST[6:0]	RW	Bit 0 : Software reset for Flush Bit 1 : Software reset for SCCB Bit 2 : Software reset for ISO FIFO Bit 3 : Software reset for OmniCE Bit 4 : Software reset for DRAM interface Bit 5 : Software reset for camera interface Bit 6 : Software reset for OV511 ⁺ & registers	00h
51h	CLKDIV[4:0]	RW	Bit 4~0 : Camera clock divisor It defines the frequency of camera clock output CCLK. CCLK is divided down based on external clock inputs CLK_48 or CLK_27. The maximum frequency of CLK_27 that OV511 ⁺ can handle is 27MHz. If both CLK_27 and CLK_48 clock inputs are enabled by pulling up pin "EN_OSC27", CLK_27 is chosen in support of camera clock. 00000 : no division (CLK_27) 11111 : CLK_27 divided by 32 If only CLK_48 clock input is enabled by pulling down pin "EN_OSC27", CLK_48 is divided by 2 and provides camera clock.	00h
52h	SNAP[3:0]	RW	Bit 0 : Hardware snapshot 0 : disabled 1 : enabled Bit 1 : Releases hardware snapshot bottom in sequence of 0,1,0 Bit 2 : Software snapshot 0 : disabled 1 : enabled Bit 3 : Snapshot status (read only)	01h
53h	EN_SYS[0]	W	Bit 0 : Software system initialization Before system is initialized, system clocks will be stopped to meet the requirement of power consumption for the whole system to be less than 100mA. After that, it can increase to max. 500mA for USB bus powered device. If pin "EN_SYSTEM" is pulled down, this bit controls system initialization. Otherwise, system is initialized right after power-on reset. 0 : system is not initialized 1 : system is initialized	00h
54h	PWCK[1:0]	RW	Bit 1~0 : Switching power clock output select 00 : 24KHz 01 : 48KHz 10 : 96KHz 11 : 192KHz	02h
55h	LEDCTL	RW	Bit 0 : LED control	00h
5Eh	USR[7:0]	RW	Bit 7~0 : User defined read/write register bits	00h
5Fh	CID[7:0]	R	Bit 7~0 : Custom ID which links to input pins "CUSTOM_ID" It is checked by the software driver to identify company names. It may be requested directly from OVT. The registered custom ID can be coded by pulling up or down resistors through pins "CUSTOM ID". If no custom ID is applied, pull-up/down resistors are also requested to avoid floating.	~

5.7 OmniCE

Table 17. OmniCE Register List

Register Address	Register Name	R/W	Function	Default Value
70h	PRH_Y[5:0]	RW	Bit 5~0 : Predication range in horizontal direction for Y channel One horizontal line is divided into horizontal segments for prediction. It defines the number of pixels contained in one horizontal segment of Y channel. Pixels in the segment except the first one are predicted by the first pixel of this segment.	1Fh
71h	PRH_UV[5:0]	RW	Bit 5~0 : Predication range in horizontal direction for UV channel	05h
72h	PRV_Y[7:0]	RW	Bit 7~0 : Predication range in vertical direction for Y channel One image frame is divided into vertical segments for prediction. It defines the number of pixels contained in one vertical segment of Y channel. Pixels in the segment except the first one are predicted by the first pixel of this segment.	06h
73h	PRV_UV[7:0]	RW	Bit 7~0 : Predication range in vertical direction for UV channel	06h
74h	QTH_Y[7:0]	RW	Bit 7~0 : Quantization threshold in horizontal direction for Y channel	14h
75h	QTH_UV[7:0]	RW	Bit 7~0 : Quantization threshold in horizontal direction for UV channel	03h
76h	QTV_Y[7:0]	RW	Bit 7~0 : Quantization threshold in vertical direction for Y channel	04h
77h	QTV_UV[7:0]	RW	Bit 7~0 : Quantization threshold in vertical direction for UV channel	04h
78h	UV_en[2] Y_en[1] CE_en[0]	RW	Bit 0 : OmniCE 0 : disabled 1 : enabled Bit 1 : Y channel operation 0 : disabled 1 : enabled Bit 2 : UV channel operation 0 : disabled 1 : enabled	06h
79h	LTEN_UV[1] LTEN_Y[0]	RW	Bit 0 : Look-up table for Y channel 0 : disabled 1 : enabled Bit 1 : Look-up table for UV channel 0 : disabled 1 : enabled	00h
80~9Fh	LT_Y	RW	Bit 7~0 : Programmable look-up table for Y channel	~
A0~BFh	LT_UV	RW	Bit 7~0 : Programmable look-up table for UV channel	~

6 USB Descriptors

The USB descriptor is a data structure with defined attributes that can respond requests from the USB host. The descriptors of OV511⁺ are hardware coded inside the chip, and no external EPROM is required.

6.1 Device

The device descriptor describes general information about OV511⁺. There is one device descriptor.

Table 18. Device Descriptor List

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	12	Size of descriptor in bytes
1	BdescriptorType	1	01	DEVICE Descriptor Type
2	BcdUSB	2	0100	USB Spec Release No.
4	BdeviceClass	1	00	Class code
5	BdeviceSubClass	1	00	Subclass code
6	BdeviceProtocol	1	00	Protocol code
7	BmaxPacketSize0	1	08	Max. packet size for enpt0
8	IdVendor	2	05a9	Vendor ID
10	IdProduct	2	A511	Product ID
12	BcdDevice	2	0100	Device release No.
14	lmanufacturer	1	00	Index of string descriptor describing manufacturer
15	lproduct	1	00	Index of string descriptor describing product
16	lserialNumber	1	00	Index of string descriptor describing the device's serial no.
17	BnumConfigurations	1	01	Number of possible configurations

6.2 Configuration

The configuration descriptor describes information about a specific device configuration. There is one configuration descriptor.

Table 19. Configuration Descriptor List

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	02	CONFIGURATION
2	WtotalLength	2	0089	Total length of data returned for this configuration
4	BnumInterfaces	1	01	No. of interfaces supported by this config.
5	BconfigurationValue	1	01	Value to use to Set Config. to select this config.
6	lconfiguration	1	00	Index of string descriptor describing this config.
7	BmAttributes	1	80	Config. char. bus powered, no remote wakeup
8	MaxPower	1	FA	Max. power consumption, 500 ma

6.3 Interface & Endpoint

The interface descriptor describes a specific interface provided by the associated configuration. There are eight interface descriptors. Each one selects one alternate setting and is followed by the corresponding endpoint descriptor.

The endpoint descriptor describes the information required by the host to determine the bandwidth requirements of each endpoint. There is no endpoint descriptor for endpoint zero.

6.3.1 Alternate 0

Table 20. Interface Descriptor List of Alternate 0

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	00	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	interface	1	00	Index of string descriptor describing this interface

Table 21. Endpoint Descriptor List of Alternate 0, Packet Size 0

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0000	Max. packet size 0
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.2 Alternate 1

Table 22. Interface Descriptor List of Alternate 1

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	01	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	interface	1	00	Index of string descriptor describing this interface

Table 23. Endpoint Descriptor List of Alternate 1, Packet Size 33

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0021	Max. packet size 33
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.3 Alternate 2

Table 24. Interface Descriptor List of Alternate 2

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	02	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code

Interface Descriptor List of Alternate 2 (continued)

6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 25. Endpoint Descriptor List of Alternate 2, Packet Size 129

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0081	Max. packet size 129
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.4 Alternate 3

Table 26. Interface Descriptor List of Alternate 3

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	03	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 27. Endpoint Descriptor List of Alternate 3, Packet Size 257

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0101	Max. packet size 257
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.5 Alternate 4

Table 28. Interface Descriptor List of Alternate 4

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	04	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 29. Endpoint Descriptor List of Alternate 4, Packet Size 385

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso

Endpoint Descriptor List of Alternate 4, Packet Size 385 (continued)

4	WmaxPacketSize	2	0181	Max. packet size 385
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.6 Alternate 5

Table 30. Interface Descriptor List of Alternate 5

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	05	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 31. Endpoint Descriptor List of Alternate 5, Packet Size 513

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0201	Max. packet size 513
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.7 Alternate 6

Table 32. Interface Descriptor List of Alternate 6

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE
2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	06	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 33. Endpoint Descriptor List of Alternate 6, Packet Size 769

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	0301	Max. packet size 769
6	Binterval	1	01	Interval for polling enpt for data transfer

6.3.8 Alternate 7

Table 34. Interface Descriptor List of Alternate 7

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	09	Size of descriptor in bytes
1	BdescriptorType	1	04	INTERFACE

Interface Descriptor List of Alternate 7 (continued)

2	BinterfaceNumber	1	00	No. of interface
3	BalternateSetting	1	07	Value used to select alternate setting
4	BnumEndpoints	1	01	No. of endpoints used by this interface
5	BinterfaceClass	1	FF	Class code
6	BinterfaceSubClass	1	00	SubClass code
7	BinterfaceProtocol	1	00	Protocol code
8	linterface	1	00	Index of string descriptor describing this interface

Table 35. Endpoint Descriptor List of Alternate 7, Packet Size 961

Offset	Field	Size	Value (Hex)	Description
0	Blength	1	07	Size of descriptor in bytes
1	BdescriptorType	1	05	ENDPOINT
2	BendpointAddress	1	81	Bit7 1 In Enpt, Bit 6..4 000, Bit 3..0 0001 Enpt No.
3	BmAttributes	1	01	Bit1..0 01 Iso
4	WmaxPacketSize	2	03C1	Max. packet size 961
6	Binterval	1	01	Interval for polling enpt for data transfer